REMARKS

Claims 1 through 4 and 6 through 24 were rejected as being obvious over Murade in view of Mattheis.

Claim 1 as previously amended calls for a plurality of substrates, each substrate having a recess. A plurality of display elements are formed on each substrate. An integrated circuit block is "mounted in the recess" on each substrate and coupled to at least one of the display elements. An integrator to couple the substrates to form a tile display.

While Murade is cited as teaching an integrated circuit block mounted in the recess, in Murade, the TFT 116 is formed in the recess. It is not a block that is mounted in the recess. It appears to be formed by integrated circuit fabrication techniques into the recess.

Thus, reconsideration of the rejection of claim 1 is respectfully requested.

Similarly, claim 12 calls for an integrated circuit block secured in the front plane. There is no integrated circuit block that is secured in the front plane in Murade or Matthies.

Therefore, reconsideration of rejected claim 12 is respectfully requested.

Claim 18 calls for forming recesses in a module to receive integrated circuit nanoblocks and depositing the nanoblocks in the recesses. There is no depositing of nanoblocks in any recesses in Murade.

Therefore, reconsideration of the rejection of claim 18 and its dependent claims is respectfully requested.

In view of these remarks, the application is now in condition for allowance.

Respectfully submitted,

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APPENDIX

1 (Previously Amended) A display comprising:

a plurality of substrates, each substrate having a recess;

a plurality of display elements formed on each substrate;

an integrated circuit block mounted in the recess on each substrate and coupled to at least one of said display elements; and

an integrator to couple said substrates to form a tiled display.

2. (Original) The display of claim 1 wherein said display element is a light emitting diode.

3. (Original) The display of claim 2 wherein said element is an organic light emitting diode.

4. (Original) The display of claim 1 wherein said integrated circuit block is a complementary metal oxide semiconductor integrated circuit.

5. (Cancelled)

6. (Previously Amended) The display of claim 1 wherein each block and said substrate are complementarily shaped.

7. (Original) The display of claim 1 wherein said block is a driver circuit for said display element.

8. (Original) The display of claim 7 wherein said block is located between a plurality of display elements.

9. (Original) The display of claim 1 wherein said block is metallized with said substrate.

10. (Original) The display of claim 1 including a ceramic back plane and a front plane including said block.

11. (Original) The display of claim 1 wherein said block is formed of a silicon substrate and said substrate is formed of glass.

12. (Original) A display comprising:

a back plane;

an optical integrator; and

a front plane between said back plane and said optical integrator, said front plane including a plurality of emissive display elements formed on said front plane and an integrated circuit block secured in said front plane and including driver circuits coupled to said display elements and to said back plane.

13. (Original) The display of claim 12 wherein said display elements are light emitting diodes.

14. (Original) The display of claim 13 wherein said elements are organic light emitting diodes.

15. (Original) The display of claim 12 wherein said block is formed of a metal oxide semiconductor integrated circuit and said front plane is formed of glass.

16. (Original) The display of claim 12 wherein said block is deposited in a recess formed in said front plane.

17. (Original) The display of claim 12 wherein said driver circuit drives a plurality of adjacent display elements.

18. (Original) A method comprising:

forming a plurality of light emitting display elements on a module;

forming recesses in said module to receive integrated circuit nanoblocks;

depositing said nanoblocks in said recesses;

electrically coupling said nanoblocks to said display elements; and

connecting a plurality of modules to form a tiled display.

19. (Original) The method of claim 18 including etching a recess in said module to receive said integrated circuit nanoblock.

20. (Original) The method of claim 18 including forming a plurality of nanoblocks by forming a sacrificial layer on a silicon substrate, etching said substrate and then finally etching said sacrificial layer.

21. (Original) The method of claim 18 including coupling said nanoblocks to circuits behind said light emitting display.

22. (Original) The method of claim 18 including coupling said nanoblocks to said circuits through bond pads on said nanoblocks.

23 (Previously Added). The display of claim 1 wherein said block is a nanoblock.

24 (Previously Added). The display of claim 23 wherein said nanoblock includes an upper surface exposed when said block is mounted in said recess, said upper surface being substantially coplanar with said substrate.